REMARKS

Claims 1-24 and 52-53 are currently pending. Claims 25-51 have been canceled. Claims 52 and 53 have been added to enhance the scope of patent coverage. The support for new claims 52 and 53 is found on page 6, lines 6 and 7, of the specification as filed. Claim 1 has been amended to correct an obvious error. Claim 16 has been amended to correct its dependency. It is respectfully submitted that no new matter has been added.

The Patent Office rejected claims 1-24 under 35 U.S.C. 112, second paragraph, as being indefinite. Claim 1 has been amended to resolve the antecedent basis of "the existence." Claim 16 has been amended to depend from claim 15. It is respectfully requested that the Patent Office withdraw its rejection of claims 1-24 under 35 U.S.C. 112, second paragraph.

The Patent Office rejected claims 1-3, 12-14, and 16-21 under 35 U.S.C. 102(e) as being anticipated by Taylor, U.S. Published Patent Application No. 2004/0230934.

For a claim to be anticipated, each and every non-inherent claim limitation must be disclosed in a reference. MPEP 2131

Claim 1 recites "A computer program product comprising program instructions stored by a computer-readable medium for directing operations of a computer during specification of an integrated circuit, comprising first computer program code that enables **a user to specify existence of uncertainty in at least one circuit**; and second computer program code that **automatically** implements the specified uncertainty as at least one programmable circuit."

The Patent Office asserted (page 2, bottom, of the Office Action mailed January 30, 2006) "(Claim 1) first computer program code that enables a user to specify the existence of uncertainty in a least one circuit (para. 0013, 0020, 0025); and second computer program code that automatically implements the specified uncertainty as at least one programmable circuit (para. 0013, 0020, 0025)."

Taylor does not disclose code that "automatically implements the specified uncertainty as at least one programmable circuit." Taylor discloses (paragraph 0013) a designer may avail of modern FPGAs' abundance of I/O pins for making ready design changes. Taylor discloses (paragraph 0020) a designer assigns programmable logic blocks of known sizes, later programmable logic blocks with unknown sizes or locations subject to change are assigned. Taylor discloses (paragraph 0025) a designer may reserve space with several FPGAs or different

spaces within one FPGA. Instead of disclosing code that automatically implements the specified uncertainty as at least one programmable circuit, Taylor appears to teach away from automatically implementing an uncertainty as a programmable circuit. Taylor discloses a prior art solution that uses automatic partitioning tools that allows a designer to input an ASIC design in which the design software may move programmable logic blocks (paragraph 0007). Taylor finds the disclosed prior art automatic partitioning tools to have problems such as arbitrary and unpredictable signal timing and long runtimes for rerouting and resynthesis functions (paragraph 0008). In Taylor, it appears that a designer may manually implement a "one or more blocks 105 that are representations of various logical circuits and/or programmable logic blocks as programmed by a designer during the design process" (paragraph 0023). Taylor discloses a system and method in which a designer may place a programmable logic block without using automatic partitioning tools (paragraph 0027). However, Taylor does not disclose or fairly suggest "computer program code that **automatically** implements the specified uncertainty as at least one programmable circuit." Thus, Taylor does not anticipate claim 1. Also, claims 2-24 are accordingly not anticipated by Taylor.

Claim 3 recites "said first computer program code implements an Uncertain Function that is used in place of a logic function or operator." The Patent Office asserted (page 3, top, of the Office Action mailed January 30, 2006) "(Claim 3 where said first computer code implements an Uncertain Function that is used in place of a logic function or operator (para 0013, 0020)." Taylor discloses (paragraph 0013) reserving I/O pins in a FPGA and reserving spaces, but does not disclose an Uncertain Function. Thus, claim 3 and dependent claims 4-11 are not anticipated by Taylor for this additional reason.

Claim 12 recites "A computer program product as in claim 1, where said first computer program code implements an Uncertain Register as a register having a programmable size within a specified range." The Patent Office asserted (page 3 of the Office Action mailed January 30, 2006) "(Claim 12) where said first computer program code implements an Uncertain Register as a register having a programmable size with a specified range (para 0006, 0011, 0020, 0022, 0029, 0032)." Taylor appears to disclose prior art difficulties with unknown block sizes (paragraph 0006), manual partitioning techniques that require a designer to know the design content and size before partitioning (paragraph 0011), assigning blocks of unknown sizes or changeable locations

(paragraph 0020), block size considerations (paragraph 0022, 0029), and placeholders for programmable blocks of unknown size (paragraph 0032), but does not disclose or fairly suggest registers or "an Uncertain Register." Thus, Taylor does not anticipate claim 12.

Claims 13, 14, 17, 18, 19, and 21 are allowable because they depend from allowable base claim 1.

Claim 16 is allowable because it depends from allowable claim 15.

The Patent Office rejected claims 4-11 under 35 U.S.C. 103(a) as being unpatentable over Taylor in view of one or more of: Huang, U.S. Patent No. 6,618,841, and Wohl, U.S. Patent No. 6,148,436.

Claims 4-11 are allowable at least because they depend from allowable claims 1 and 3.

Claim 7 recites "said first computer program code implements an Uncertain Function Assertion for imposing at least one constraint on the Uncertain Function." Taylor discloses (paragraph 0034) pipeline latency to allow portions of the backplane of an FPGA to run at higher clock frequencies. Huang discloses (col. 7, lines 10-41) non-assignable signal that may be propagated according to logic functions in a non-assignable truth table. Wohl discloses (col. 9, line 38+, col. 14, line 26+) logic functions. Claim 7 depends upon claim 3 which recites that "said first computer program code implements an Uncertain Function that is used in place of a logic function or operator." Thus, claim 7 is not made obvious by Taylor in combination with either Huang or Wohl. Accordingly, claims 8-10 are not made obvious because they depend from claim 7.

The Patent Office is respectfully requested to favorably consider and allow all of the pending claims 1-24 and 52-53 as now presented for examination. An early notification of the allowability of claims 1-24 and 52-53 is earnestly solicited.

Respectfully submitted:

Walter J. Malinowski March 1, 2006

Walter J. Malinowski Date

Reg. No.: 43,423

Customer No.: 29683

HARRINGTON & SMITH, LLP

4 Research Drive

Shelton, CT 06484-6212

Telephone: (203)925-9400, extension 19

Facsimile: (203)944-0245

email: wmalinowski@hspatent.com

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